Sun Microsystems, Inc. Mailstop UNWK20-310 7788 Gateway Boulevard, Bldg. 20 Newark, CA 94560

July 15, 2005



Jason P. McDevitt, Ph.D Director, Technology Transfer Office College of William and Mary Corner House, 402 Jamestown Road P.O. Box 8795 Williamsburg, VA 23187-8795

Dear Mr. McDevitt,

In response to your request, Sun provides the following:

Sun MicroSystems, Inc. has applied the permutation-based memory interleaving technique, called "XOR interleaving" or "permutation interleaving", as proposed by Zhao Zhang (Ph.D.'02), Zhichun Zhu (Ph.D.'03), and Xiaodong Zhang (Lettie Pate Evans Professor of Computer Science and the Department Chair) at the College of William and Mary, in the Sun UltraSPARC® IIIi processor.

A paper about this technique entitled "A permutation-based page interleaving scheme to reduce row-buffer conflicts and exploit data locality" was published in the 33rd Annual IEEE/ACM International Symposium on Microarchitecture (Micro-33, pp. 32-41, Monterey, California, December 10-13, 2000). A chief finding demonstrated in the report by the three researchers was that address mapping conflicts at the cache level, including address conflicts and write-back conflicts, may inevitably propagate to the DRAM memory under a standard memory interleaving method, causing significant memory access delays. The proposed permutation interleaving technique proposed a low cost solution to these conflicts problems.

This statement is an acknowledgment of Sun's use of the technique for Sun's purposes and is neither an endorsement of the technique nor recommendation of its use by others.

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Very truly yours,

Marc Tremblay

Sun Fellow, Vice President & Chief Architec≰